NEW TOPOLOGY OF CASCADED HYBRID MULTILEVEL INVERTER

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Abstract - **In this paper, a new topology of cascaded multilevel inverter using a reduced number of switches is proposed. The new topology has the advantage of reduced number devices compared to traditional configurations and can be extended to any number of levels. This topology results in reduction of installation area, cost, computational time and has simplicity of control system. This structure consists of series connected sub-multilevel inverter blocks. The GA technique finds the optimal solution set of switching angles, if it exits, for each required harmonic profile. Both simulation results and experimental verification of the proposed inverter topology for different number of levels and different harmonic profiles are presented.**

Keywords**: Multilevel inverter, Cascaded multilevel inverter, H –bridge, Full-bridge, Sub-multilevel inverter, Selective harmonic elimination, Programmed PWM, Genetic algorithms.**

I. INTRODUCTION

A Multilevel inverter is a power electronic system that synthesizes a desired output voltage from several DC voltages as inputs. The concept of utilizing multiple small voltage levels to perform power conversion was presented by a MIT researcher. Advantages of this approach include good power quality, good electro-magnetic compatibility, low switching losses and high voltage capability. The first introduced topology is the series H-bridge design. This was followed by the diode clamped inverter which utilizes a bank of series capacitors to split the dc bus voltage. The flying-capacitor (or capacitor clamped) topology uses floating capacitors to clamp the voltage levels. Another multilevel design, involves parallel connection of inverter phases through inter phase reactors. One particular disadvantage of multilevel inverter is the great number of power semi-conductor switches needed. So, in practical implementation, reducing the number of switches and gate driver circuits is very important. Genetic algorithms (GAs) are stochastic optimization techniques. Genetic Algorithms are applied in this to compute the switching angles in a cascaded multilevel inverter to produce the required fundamental voltage while, at the same time, 3rd and 5th harmonics are reduced. It is shown in that the problem of harmonic elimination is converted into an optimization task using binary coded genetic algorithms (GA).Various components of GAs such as chromosomes, fitness function, reproduction, crossover and mutation are illustrated as applied to the present work.

II TOPOLOGY

Fig1 shows the suggested basic unit for a sub-multilevel inverter. This consists of a capacitor (with dc voltage equal to V_{dc}) with two switches S_1 and S_2. Table 1 indicates the values of V_o for states of switches S_1 and S_2. It is clear that both switches S1 and S_2 cannot be on simultaneously because a short circuit across the voltage V_{dc} would be produced. It is noted that two values can be achieved for V

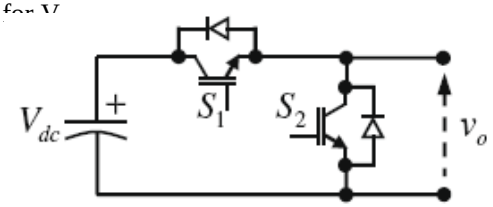

Fig 1. Basic unit for a sub-multilevel inverter

State	Switches states		
	s_1	s_2	$\mathbf{v_o}$
1	on	off	V_{dc}
2	off	on	0

Table I Values of v_o for states of switches s_1 and s_2

The basic unit shown in Fig. 1 can be cascaded as shown in Fig. 2

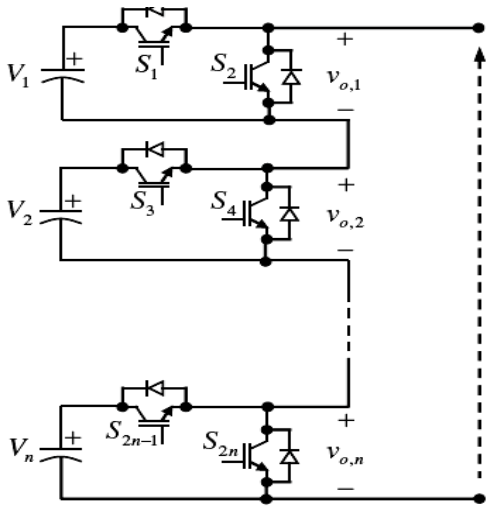

Fig 2. Sub-multilevel inverter in a cascaded form

State	Switches states							v_0
	S_1	S_2	S_3	S_4	⋯	S_{2n-1}	S_{2n}	
1	Off	On	Off	On	⋯	Off	On	0
2	On	Off	Off	On	⋯	Off	On	v_1
3	Off	On	On	Off	⋯	Off	On	v_2
4	On	Off	On	Off	⋯	Off	On	V_1+V_2
⋮	⋮	⋮	⋮	⋮	⋯	⋮	⋮	⋮
2^n	On	Off	On	Off	⋯	On	Off	$\sum_{i=1}^{n} v_1$

Table II I Values of v_o for states of switches s_1 and s_2

The output voltage of conventional multilevel inverter for all times has zero or positive value. In the following, we propose a new method for determination of magnitudes of dc voltage sources which are used in the proposed multilevel inverter.

The number of maximum output voltage steps of the n series basic units can be evaluated by, Nstep=n+1 The maximum output voltage is given by, $Vo_{,max}=n*V_{dc}$

III. HYBRID TOPOLOGY

Power Circuit

The considered hybrid topology is composed by a traditional three-phase, three-level NPC inverter, connected with a single phase H-bridge inverter in series with each output phase. The power circuit is illustrated in Fig. 1, with only the H-bridge of phase a shown in detail. For testing as an inverter, the DC source for the NPC converter is provided by two series connected diode bridge rectifiers, arranged in a twelve-pulse configuration. The H- bridge DC-links are not connected to an external DC power supply, and they consist only of floating capacitors kept at a constant voltage by the control strategy detailed in this Section.

In the hybrid topology considered, the NPC inverter pro- vides the total active power flow. For high-power medium voltage NPC, there are advantages to using latching devices such IGCTs rather than IGBTs, due to their lower losses and higher voltage blocking capability, imposing a restriction on the switching frequency. In this work, an NPC operating at a low switching frequency (of 250Hz) is considered. In contrast, the H-bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. This calls for the use of IGBT.

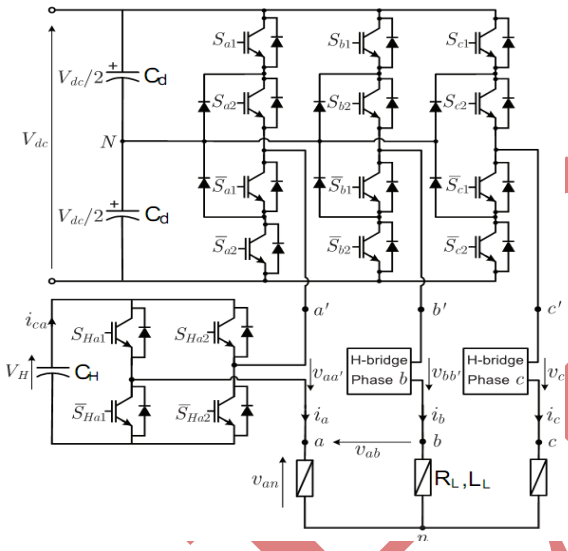

Fig. 3. Hybrid topology power circuit.

The proposed converter, shown in Fig.3, can be analyzed from two different points of view. The first interpretation is as a single hybrid multilevel inverter with a nine level phase voltage, achieved by the cascade connection of a three level NPC leg and an H-bridge per-phase. The second interpretation is as an NPC converter with a series active filter that compensates for the harmonic content introduced by the low switching NPC stage. If the NPC bridge is to be modulated at a low switching frequency, as proposed in this work, the second interpretation would seem to be more appropriate to devise a control algorithm, leading to the following two design challenges:

- To determine the lowest value of H-bridge dc-link voltage (VH) that achieves adequate voltage harmonic compensation.
- To devise a control algorithm that ensures that the floating dc-links are properly regulated at this value.

For the modulation of the NPC inverter, the Selective Harmonic Elimination (SHE) method has been selected. This method has the advantage of very low switching frequency and hence low switching losses, while eliminating the low order harmonics. With the use of SHE modulation, the fundamental output voltage of the converter is synthesized by the NPC converter and thus the series HBs will only need to supply reactive power, allowing for operation with floating capacitor DC-links.

A drawback of any synchronous modulation method, such as SHE, is its limited dynamic capability and poor closed loop performance due to the use of a pre-calculated lookup table based approach, rather than real time calculations. These drawbacks can, to a large extent, be overcome by the use of the series H-bridges which are modulated in real time, introducing

an additional degree of control freedom to the circuit and cleaner feedback signals.

IV. NPC SELECTIVE HARMONIC ELIMINATION

Three-level SHE is an established and well documented modulation strategy A qualitative phase output voltage waveform is considering a 5-angle realization, so five degrees of freedom are available. This enables the amplitude of the fundamental component to be controlled and four harmonics to be eliminated. Since a three-phase system is considered, the triple harmonics are eliminated at the load by connection, and hence, they do not require elimination by the modulation pulse pattern. Thus, the 5th, 7th, 11th and 13th harmonics are chosen for elimination. For line-connected applications, this 5-angle implementation results in a switching frequency of 250Hz for the NPC portion of the converter and leaves the 17th as the first harmonic component to appear in the steady state load current. On the other hand, for

variable frequency drive applications, the number of angles must be varied in order to maintain a near constant switching frequency at any operation point.

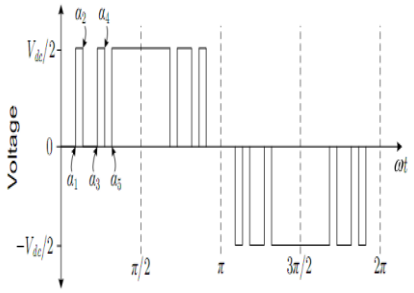

Fig. 4. Wave form

V. CASCADED H-BRIDGE MULTILEVEL INVERTERS (CHB-MLI)

An alternative multilevel inverter topology with less power devices requirement compared to previously mentioned topologies is known as cascaded H-bridge multilevel inverter (CHB-MLI) and the topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. Owing to this property, CHB-MLIs have also been proposed to be used with fuel cells or photovoltaic arrays in order to achieve higher levels.

The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generates three voltage levels as $+V_{dc}$, 0, $\_V_{dc}$ by connecting the DC source to the AC output by different combinations of four switches, S_{A1}, S_{A1} 1, $S_{A\ 2}$, and S_{A2} 1 as seen in first cell of Fig. 5. The CHB-MLI that is shown in Fig. 5 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain $+V_{dc}$, S_{A1} and S_{A2} 1 switches are turned on, whereas _Vdc level can be obtained by turning on the $S_{A\ 2}$ and S_{A1} 1. The output voltage will be 0 by turning on S_{A1} and S_{A2} switches or S_{A1} 1 and S_{A2} switches. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase. The switching states of a CHB-MLI (sw) can be determined, by) m ¼ 2n þ 1 ð4Þ sw ¼ 3m ð5Þ The first leg phase voltage (Van) of Fig. 5 is constituted by multiplying Va1 and Va2 values of series connected H-bridge cells and will generate a stepped waveform as seen in Fig. 6. Positive output pulses are shown with P_1 and P_2 while the negative ones are indicated as P_1 1 and P_2 .1. The Fourier series expansion of the general multilevel and the transform is applied for Fig. 5, where is the harmonic number of the output voltage of inverter. The switching angles that are indicated as H1 . . .H5 can be chosen to obtain minimum voltage harmonies and several fundamental frequency switching techniques evaluated such as selective harmonics eliminations PWM or active harmonic elimination PWM.

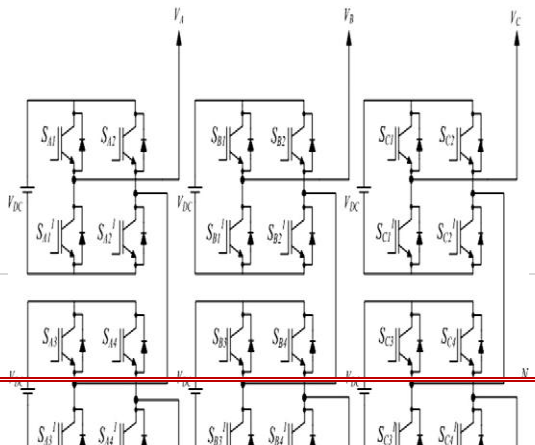

Fig.5. Three-phase five-level topology of cascaded H-bridge multilevel inverter

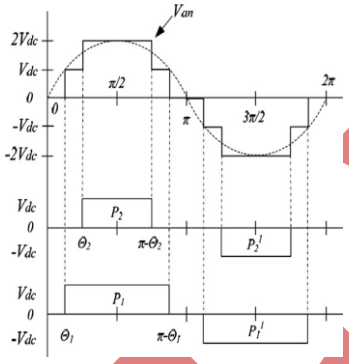

Fig.6.. Phase output voltage waveforms of a five-level topology CHB-MLI with two separate DC sources.

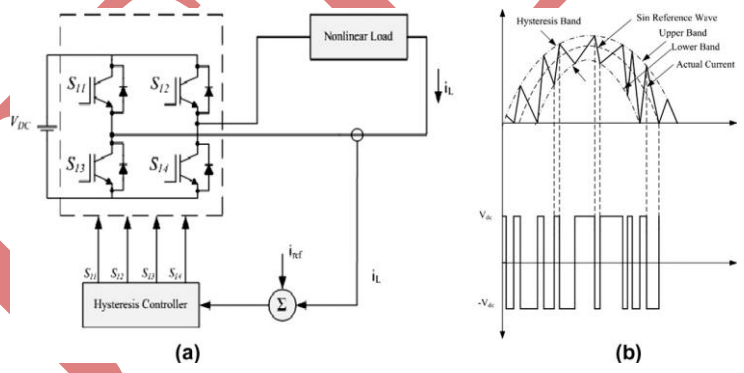

Fig.7. Hysteresis current control: (a) block diagram of a H-bridge cell with hysteresis controller, (b) hysteresis current band and voltage curves of load feedback.

VI. COMPARISON OF MULTILEVEL INVERTER TOPOLOGIES AND CONTROL SCHEME

The most common multilevel inverter topologies and control schemes have been reviewed in this paper. The multilevel concept has been introduced with a diode clamped topology in 1980s by Nabae. MLIs are increasingly being used in medium voltage and high power applications owing to numerous advantages such as low power dissipation due to reducing the voltage stress on switching devices and minimizing the harmonic contents at the output of the inverter. The selected control scheme for an MLI determines the affectivity on harmonic elimination, while generating the ideal output voltage. The applications of MLIs including induction machine and motor drives, active filters, renewable energy sources interconnection to grid, flexible AC transmission systems (FACTS), and static compensators (STATCOM) have been widely used in industrial applications. Although the variety of MLI applications, there are several limitations have been

discussed for topologies and control schemes. DC-MLIs ,especially three-level structure, have a wide popularity in motor drive applications besides other multilevel topologies due to reducing THD with robust control of SHE-PWM control scheme. However, it would be a restriction of complexity and pre-defined switching angles when the level exceeds the three. The SPWM and SVM modulation techniques succeed this limitation of DC-MLI for higher level topologies. Other applications of DC-MLI can be defined as active filters and STATCOM in high voltage grid interconnections.
The most appropriate control schemes with application matching according to selected multilevel inverter topology. The sign of bolded check means the proper matching between topology and control scheme or topology and application. The plain checks have been used to emphasize that there are some studies given in the literature about these applications but does not provide proper solutions.

The bolded double check shows the most appropriate selection, while the cross defines the undesirable matching about harmonic reducing or affectivity issues. The DCMLIs are efficient in fundamental frequency switching applications such SHE-PWM and SVM, but the SVM will cause to an increment on voltage and current THD in the increased number of clamping diode conditions. The FC-MLI topology that has been introduced in 1992 is similar to DC-MLI except utilizing DC side capacitors instead of clamping diodes in a ladder form. The FC-MLI is the unique topology that requires the most switching and auxiliary devices to generate a staircase output voltage. The increment of level will cause to increase auxiliary capacitor number and restrain the accurate charging and discharging control of capacitors, hence designer will be encountered with the requirement of a pre-charge controller system. Although these disadvantages, the most important advantages of FC-MLI topology are preventing the filter demand, and controlling the active and reactive power flow besides phase redundancies. The FC-MLI topology is mostly used in motor drive and active filter applications with SHE-PWM or phase shifted PWM control methods. The CHB-MLI has the least components for a given number of levels according to topologies discussed before. The CHB-MLI topology consists of a series of H-bridge cells to synthesize a desired voltage from SDCSs which may be obtained from batteries or fuel cells. All these properties of cascade inverters allow using various pulse width modulation (PWM) strategies to control the inverter accurately. CHB-MLIs have been previously designed for static VAR compensators and motor drives, but the topology has been prepared an interface with renewable energy sources due to using separate DC sources. There are numerous studies have been performed on CHB-MLIs for connecting renewable energy sources with grid and power factor correction. The SPWM control scheme
is mostly being used in the control of CHB-MLI due to simplified design considerations according to SVM.

Fig.7. SDM control of a multilevel inverter

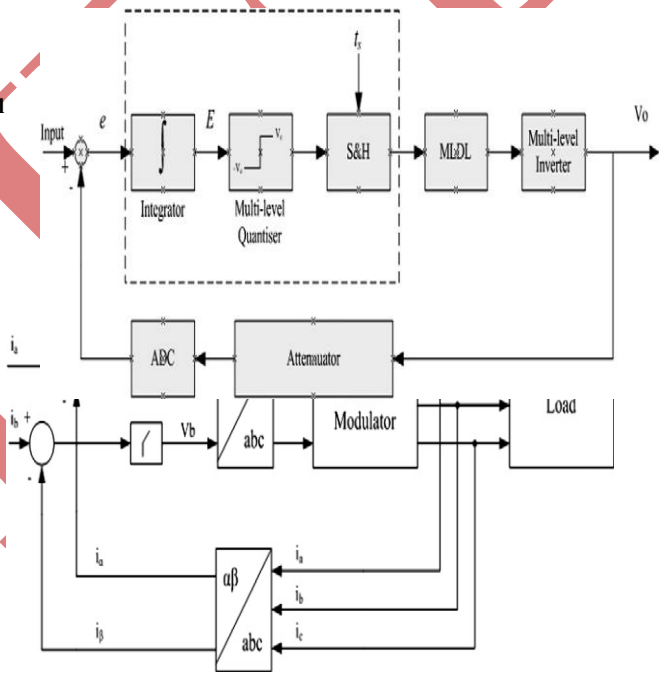

Fig. 8. The block diagram of stationary linear current controller

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VII. CONCLUSION

Based on the survey of conventional multilevel inverter topologies given in the previous sections, general and asymmetrically constituted H-MLIs have been also reviewed in this paper. Many new hybrid topologies can be designed through the combinations

of three main MLI topologies. Besides the combination of topologies, the trade-offs in MLI structures can be dealt by using AH-MLIs that is formed using different DC source levels in inverter cells. Nevertheless, conventional PWM strategies that generate switching frequency at fundamental frequency are not appropriate for AH-MLIs due to switching devices of the higher voltage modules

would have to operate at high frequencies only using some inverting instants. To achieve this control strategy, hybrid modulation methods have been proposed that provide to get higher power cells switched at low frequency and low power cells switched with high frequency. The detailed researches show that the general idea of modulation strategies based on multi-carrier SPWM such as PD,POD, and APOD can be utilized for hybrid topologies.

Due to numerous applications of conventional MLIs and flexibility to design the hybrid MLI topologies, this paper cannot cover all utilizations with MLIs, but the authors intend to provide a useful basis to define the most proper control schemes and applications as depicted in . In addition to these, the fundamental design and control principles of MLIs have been introduced as a result of a detailed literature survey. This paper has been destined to provide a reference to readers and the results given in this paper can also be extended with experimental studies.

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