

A TECHNICAL REVIEW ON CAPACITOR BANK SWITCHING WITH VACUUM CIRCUIT BREAKERS

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ABSTRACT

After interruption of a capacitive current sometimes Non Sustained Disruptive Discharges (NSDD's) are observed when using vacuum circuit breakers. According to network calculations, NSDD's generate significant over-voltage on the terminal of the capacitor bank to earth and across the circuit breaker (CB) terminals. In a full scale experiment at 12kV on an 8MVar capacitor bank artificial NSDD's are produced using a TVG. The over-voltage depends on the momentary voltage difference across the breaker and, hence, varies with the phase angle. The over-voltage on the terminal of the capacitor bank to earth varies from 1.5 to 4.2 pu, and to maximum 5.2 pu. across the CB terminals. The effectiveness of surge arresters on the limitation of the over-voltages is measured. The over-voltages are limited to 2.2 pu. on the terminals of the capacitor bank to earth and 3.2 pu. across the CB terminals. A single surge arrester on the neutral point of the capacitor bank yields the same level of protection and, therefore, is a cost effective alternative.

I. INTRODUCTION

The capacitive current switching duty is characterized by frequent, day to day or hour by hour, switching of low to moderate currents in industrial or public networks, and by a low rate of rise of recovery voltage. Modern circuit breakers (CBs) which claim a long mechanical but also electrical life without maintenance seem to be best adapted to this switching duty [1,2,3]. Yet the behavior of vacuum CB's is rather different from that of gas CB's.

SF6 CBs, in the past referred to as "restrike free" breakers, are according to the new IEC62271-100 class C2 breakers with proven "very low" restrike probability [4]. Field experience indicates that the restrike probability even for the electrically very stressed 36 kV networks is lower than 1/50.000.

For vacuum CB's, the physical processes during the capacitive switching duty have been studied by [5]. They found that the pre-ignition at contact closing and the subsequent inrush current heavily eroded the contacts leading to detached particles. These particles cause late breakdowns which appear as NSDD's.

* NSDD or non-sustained disruptive discharge [7] is a disruptive discharge associated with current interruption that does not result in the resumption of power frequency current or, in the case of capacitive current interruption does not result in current in the main load circuit.

Breakdown frequencies of typically 3/1000 were found under the experimental conditions studied.

A restrike can generate an overvoltage of 3 pu. between the terminals of the capacitor bank, whereas a NSDD is accompanied by a sudden voltage shift of the neutral capacitor bank voltage, which leaves the voltage across the

capacitor unchanged, but creates an overvoltage of between 1.5 and 5 pu. on the terminal of capacitor bank to earth. Due to the rare occurrence and the random nature of the phenomenon, the relation between NSDD and overvoltage is not well understood. First in section II this question is addressed using a numerical network simulation. By this the worst case overvoltage for different voltage levels is determined. Then in section III an experiment designed to verify the simulation results is shown. Here the NSDD is created artificially, which permits to measure the influence of phase angle and network parameters. A good understanding of the origin of the overvoltage enables the definition of protective measures adapted to the switchgear and capacitor bank. Finally in section IV protection schemes based on surge arresters are tested and compared on their effectiveness.

II. ORIGIN OF OVERVOLTAGES

2.1 Numerical Simulation

The simplified electrical circuit, fig. 1, will be used here to simulate the phenomena associated with a NSDD; the NSDD is simulated as a temporary loss of dielectric strength in the vacuum interrupter of a vacuum CB.

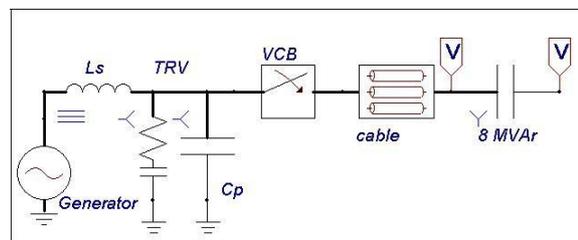


Fig. 1 : Electric Circuit used to Calculate Overvoltage on Capacitor Bank During a NSDD.

The source side of the network is represented by:

- a generator with a driving voltage of U
- a short circuit impedance of value L_s
- a TRV network as defined by IEC for short circuit conditions
- a capacitor to account for parallel feeders

The load side of the network is represented by:

- a 8MVAR capacitor bank with floating neutral
- single phase cables between CB and the bank.

The load and the source side of the network are connected to each other by the CB. The CB is treated as an ideal breaker with a NSDD some time after current interruption. The moment of NSDD has been chosen in order to create the worst possible case. The CB is allowed to recover immediately at the first occurring current zero. Parasitic capacitance's on both sides of the CB have been neglected intentionally as they tend to mask the dominant process. [1] At a NSDD, on the middle phase for the case illustrated by fig. 2, the voltage across the breaker moves as a travelling wave through the line impedance towards the capacitor bank. The capacitor bank being a high frequency short circuit allows the wave to pass on to the neutral point of the bank. At the neutral point the wave splits itself and continues its propagation in the neighbouring phases towards the healthy CB poles. These healthy poles are in fact open terminals for the incoming wave causing it to reflect by doubling the voltage. After reflection the wave travels back to the failing CB pole. Here it creates a current zero passage on which the breaker can interrupt. The frequency of this current is typically of the order of 100 kHz for cable

connected capacitor banks. Fig. 2 shows the voltage swing to earth on the bank terminals. Note that

- For each of the three bank terminals the voltage jumps to a new value, which means that the neutral point of the bank attains also a different value.
- The voltage difference between terminals remains unchanged. The capacitors themselves are not stressed by the breakdown.

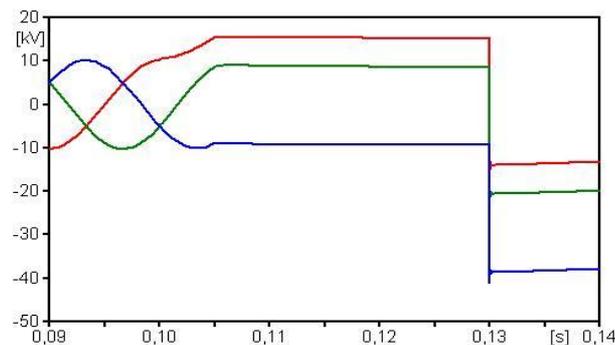


Fig. 2 : The Voltage on all 3 Capacitor Bank Terminals During Current Interruption (at 0.1s) Followed by a NSDD (at 0.13s) in a 12kV Network.

- The maximum terminal voltage to earth attains a high value see table I. This is a DC voltage, so all parts of the installation are stressed during a long period.
- The CB is stressed by the composed voltage of network voltage and capacitor bank terminal voltage.
- The capacity of the bank itself is of no significance for the phenomenon.

Table 1: Compilation of Voltages Associated with Capacitor Bank Switching for Nominal Network Voltages

U_n kV _{eff}	U_S kV _{eff}	U_{C-banc} kV	U_{CB} kV	BIL kV	Power frequency kV _{eff}
12	10	47	55	75	28
24	20	93	110	125	50
36	30	140	164	170	70

2.2 Identification of Zones at Risk

In table I the maximum possible overvoltage produced by a NSDD is shown for three commonly used classes of network voltages. For each voltage class column 2 gives U_S the nominal network voltage. Column 3 gives the maximum overvoltage on the capacitor bank terminal to earth and column 4 the maximum overvoltage across the CB terminals. For reference the BIL and power frequency withstand voltages of the equipment are given. For all three voltage classes both overvoltages exceed the peak value of the power frequency withstand voltage. For the CB the overvoltage comes very close to the rated BIL voltage for 36 kV class networks.

III. EXPERIMENTAL VERIFICATION

3.1 Test Procedure

The objective was to create in a reproducible way NSDD type of breakdowns in a capacitive current interruption test. This allowed to minimize the number of tests to obtain a NSDD as in normal switchgear this phenomenon is rare and very irreproducible, and to have the measurement window set around the breakdown for precise measurement. A triggered vacuum gap (TVG) parallel to the R-phase of the VCB is used to create an artificial NSDD in a controllable way.

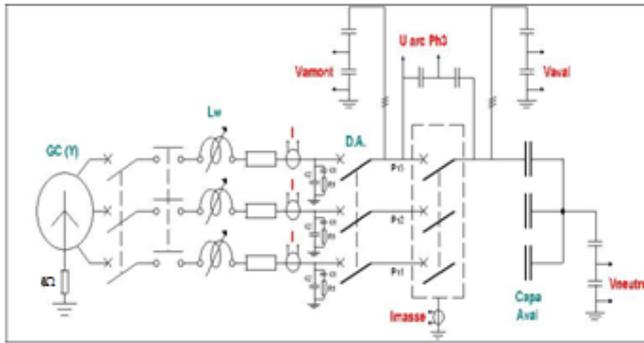
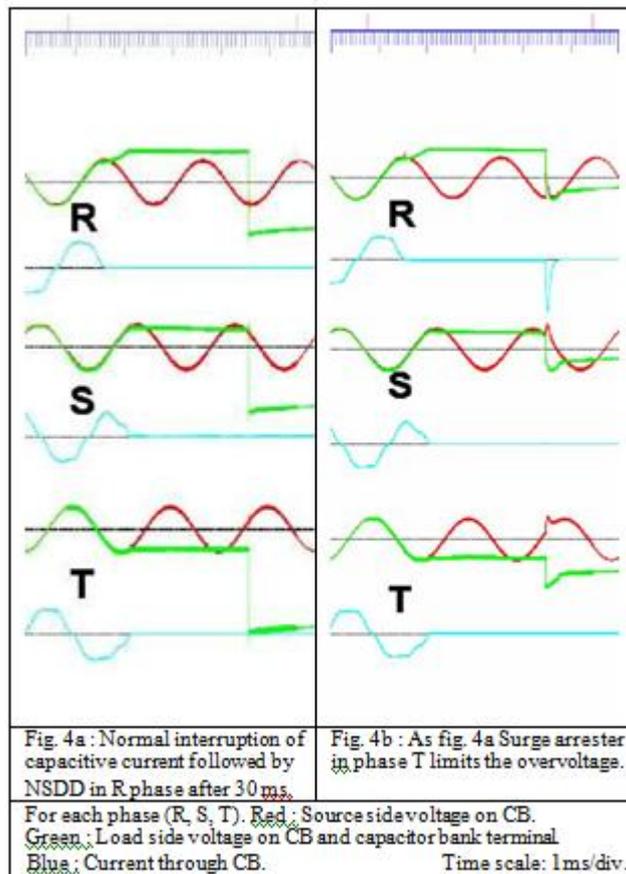


Fig. 3 : 3-phase test circuit with generator and 8 MVA capacitor bank.

TABLE II : Main characteristics of test system

Capacitive circuit directly fed by generator		
Nominal voltage	12.1	kV
Nominal current	430	A
Short circuit current	14.7	kA
TRV circuit		
rise time t3	61	Js
peak voltage	23	kV
Capacitor bank	184	JF/phase
Cable connection	30	Metres
C cable	10	nF
Short circuit inductance		
Lw	1,51	mH
R	<30	mOhm
Test object : VCB : 12 kV 25 kA 1250 A (A.E. in fig. 3) Triggered Vacuum Gap on phase R		



A separate experiment confirmed that the TVG was able to interrupt currents of 300A at 100kHz and 10 A at 900 kHz at the first current zero. Hence, the duration of the “artificial” NSDD is determined by the circuit topology and only one half cycle of current will pass through the TVG. The characteristics of the test circuit

are given in fig. 3 and table II.

3.2 Test Results

Fig. 4a shows an oscillogram of a normal interruption. The first phase to interrupt, R, creates a constant voltage on the capacitor bank terminal of 1.5 pu. Then 30 milliseconds after current interruption the NSDD is generated at a maximum voltage difference across the CB. At this moment the voltage on the C-bank terminals changes suddenly and settles to a new constant value. The highest overvoltage is in phase T.

The instant of occurrence of the NSDD was varied by firing the TVG at a predetermined moment to see the influence of the phase angle on the nature and the value of the over-voltage. Fig. 5 shows the measured voltage on the capacitor bank terminal in phase T after the NSDD in phase R. Before the NSDD the voltage is about 0.89 pu. The voltage jump is between 0.6 and 3.2 pu. leading to an over-voltage of maximum 4.1 pu. Similar results are obtained when the NSDD occurs in the second or third phase to interrupt, although the maximum overvoltage is slightly lower : 4.0 pu.

Note that the over-voltage is the addition of the original capacitor bank voltage after current interruption and a voltage jump due to the NSDD. The amplitude of the voltage jump depends on two factors :

- the voltage across the breaker at the instant of breakdown, which varies with time or phase angle, and which is maximum 2.5 pu. (see fig. 4a).
- an amplitude multiplication (K-)factor which is here about 1.3

The voltage difference at breakdown is transmitted integrally to the neighbouring phases as predicted by the numerical simulation. Except for a reduced amplitude factor the behaviour found is identical to the simulation.

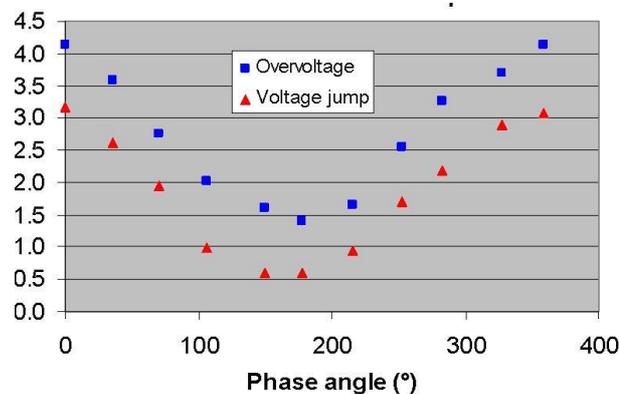


Fig. 5 : Variation of over-voltage expressed in pu due to instant of occurrence (phase angle) of the NSDD in 1st phase to interrupt. Estimated amplitude factor of 1.3.

3.3 Influence of TRV circuit

The influence of the TRV circuit on the high frequency behaviour of the breakdown has been studied with the following circuits :

TRV-1 : The standard TRV circuit composed of 2 branches see fig. 1.

TRV-2 : No TRV circuit; only stray capacitance between Generator and CB.

TABLE III

	TRV-1	TRV-2
Voltage jump		
K-theoretical	2	2
K-Immediate	1.6	1.7
K-Late	1.3	1.6
Damping time	16.5Js	13.5Js
Frequency NSDD		
current	150 kHz	28 kHz
Current	28 A	6 A

Results are shown in table III. The voltage jump after breakdown can be characterized by :

- A peak voltage immediately after the NSDD: with K factor : K-immediate.
- A dc voltage after a transition period: K-late. The transition is characterized by a time constant here called “damping time”.
- The frequency of the breakdown current.

Fig. 6 shows an oscillogram of the voltage across the CB during the NSDD for TRV-2 circuit.

Numerical simulation suggests voltage doubling with a K-factor equal to 2. Therefore the reduced value of K-immediate is attributed to damping of the high frequency current at NSDD.

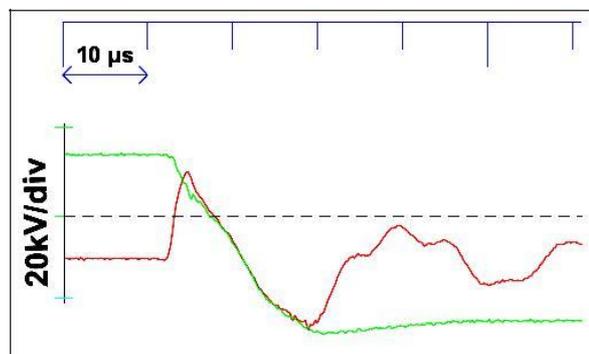


Fig. 6 Zoom at voltage behaviour at NSDD in R phase with TRV-2. Green : Load side voltage on CB and capacitor bank terminal. Red : Source side voltage on CB. Time scale 10Js/div.

IV. PROTECTION BY SURGE ARRESTERS

Arresters are commonly proposed as means to protect the capacitor bank against excessive overvoltages due to restrikes [6]. In such a case the overvoltage rise-time is of the order of milliseconds. Yet in case of an NSDD the overvoltage rise-time is only several microseconds. In order to verify the effectiveness of the surge arrester the following two cases are investigated

4.1 Surge Arresters on all Three Phases to Earth

Test conditions are similar as under section IIIA but with surge arresters on the load side of the CB to earth. On initiation of a NSDD in phase R, the highest overvoltage was in phase T with immediate limitation of this overvoltage by the surge arrester in phase T (fig. 4b). A significant current flows through the surge arrester: 890 A during 1 ms; representing an energy of about 6 kJoule. This current is determined by :

1. The series impedance of two branches R and T of the capacitor bank and the series inductance of phase R and the resistance to ground of the generator.
2. The voltage difference across the capacitor prior to breakdown minus the voltage of the arrester

4.2 Surge Arrester on Neutral to Earth

Test conditions are similar as under section IIIA but with a single surge arrester on the neutral point of the capacitor bank. If a NSDD was initiated in phase R, the highest overvoltage was in phase T with immediate limitation of this overvoltage by the surge arrester. A significant current flows through the surge arrester: 575 A during 2.5 ms; representing an energy of about 6 kJoule. This current is determined by

1. The series impedance of one branch of the capacitor bank, the inductance of one phase of the circuit and the resistance to earth of the generator.
2. The voltage difference across the capacitor prior to breakdown minus the voltage of the arrester

V. DISCUSSION

The main results of this study are summarized in table IV. An important difference is found between the numerically and experimentally obtained overvoltage values. The measured overvoltage on the banc terminal to ground is significantly lower than calculated due to damping elements in the circuit. The peak over-voltage has a limited duration of about 10Js. Surge arresters effectively limit the overvoltage to values as low as 2.2 pu between terminal and earth. The capacitors themselves are not stressed either by the NSDD or by the action of the surge arresters during limitation. The dimensioning of the surge arrester should take into account the energy of the discharge current during a NSDD.

TABLE IV : Over-Voltages in Capacitor Bank Switching

Situation		Capacitor bank terminal	Across CB
1	Normal Interruption	1.5 pu	2.5 pu
2	NSDD : Predicted	6.0 pu	7.0 pu
3a	NSDD (K-Late = 1.3)	4.2 pu	5.2 pu
3b	NSDD (K-Immediate = 1.7)	5.2 pu	6.2 pu
4	Surge arresters on all terminals	2.2 pu	3.2 pu
5	Surge arrester on C-bank neutral	2.2 pu	3.2 pu

VI. CONCLUSION

This study focussed on the interaction of vacuum circuit breaker with a capacitor bank during switching operation. The occurrence of a Non Sustained Disruptive Discharge leads to a shift of the voltage of the neutral point of the bank. Although the phenomenon in itself is rare, the over-voltages produced are deterministic and depend on the recovery voltage of the phase in which the NSDD occurs and on the moment of breakdown. The experimental study shows that the overvoltage after NSDD is limited to about 4.2 pu. on the capacitor bank terminals. Surge arresters are shown to be an effective means to limit this overvoltage. As cost efficient solution it is proposed to use a single surge arrester on the neutral point of the capacitor bank.

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