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A Low Power Timing Error Tolerant CircuitBy Controlling A Clock

Mrs. P. Venukumari[1], G. S. M. Lakshmi[2], G. Gayathri[3], G. Kiran Kumar[4], A. Gopichandu[5]

Asst.Prof[1], Students[2-5],

Tirumala Engineering College, Narasaraopet, Andhra Pradesh, India

ABSTRACT

This project presents clock controlling technique in flip flops to prevent timing errors. Timing errors are detected and corrected by modify the clock of flip flop without changing the system clock with minimum logics. Timing error is now getting increased attention due to the high rate of error-occurrence on semiconductors. Even slight external disturbance can threaten the timing margin between successive clocks since the latest semiconductor operates with high frequency and small supply voltage. To deal with a timing error, many techniques have been introduced. Nevertheless, existing methods that mitigate a timing error mostly have time-delaying mechanisms and too complex operation, resulting in a timing problem on clock-based systems and hardware overhead. In this article, we propose a novel timing-error-tolerant method that can correct a timing error instantly through a simple mechanism. By modifying a clock in a flip-flop, the proposed system can recover a timing error without the loss of time in the clock-based system. Furthermore, due to the compact mechanism, the proposed system has low hardware overhead in comparison with existing timing-error-tolerant systems that can recover the error instantly.

1. INTRODUCTION

Timing errors are an increasing reliability concern in nanometre technology, high complexity, and multi-voltage\frequency integrated circuits. A local error detection and correction technique is presented in this work that is based on a new bit flipping flip-flop. Whenever a timing error is detected, it is corrected by complementing the output of the corresponding flip-flop. The timing-error rate is increased as the clock frequency is increased. Since the clock period is getting minimized, critical paths in the circuit are susceptible to timing errors. Furthermore, variations on the CMOS process, power supply, and temperature impact the performance of modern integrated circuits, which results in the high incidence of timing errors. As the supply voltage decreases, the delay of the circuit can drastically change between the typical case and the worst case of process, voltage, and temperature conditions. Process variability in device and circuit parameters is one of the primary challenges currently faced by the semiconductor industry. Besides static variations that occur during chip fabrication, dynamic parameter variation – resulting from environmental and workload changes – is also possible

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during the chip's operation. Examples of dynamic variations include supply voltage droops, temperature changes, and transistor aging degradation. Variations change the circuit's characteristics in terms of timing and power consumption, and, thus, if not appropriately handled, they may adversely impact performance, power, and the system's overall reliability. With the 0.4-V operation, the logical path with the worst case is 12x slower than that with the typical case. Moreover, transistor aging issues are critical for the occurrence of timing errors. Due to the negative-bias temperature instability (NBTI) in CMOS, the threshold voltage is lowered, which finally increases the path delays of logics. Hence, a timing-error- tolerant method is highly required in order to implement reliable systems. Error tolerance refers to the ability of a system to function even after an error has occurred. In other words, an error tolerant system is one in which the results of making errors are relatively harmless.

The timing error occurs because of the delay in combinational circuits that are located between the memory elements. After the edge of the clock, the delayed data cannot be stored in the memory element properly. To deal with the timing error, many related methods have been proposed. One of the representative methods of timing-error-tolerant systems is the temporary error- detection system. By comparing the output of a flip-flop with a delayed output, it detects the transient timing error that is propagated from the input with low hardware overhead. However, it only detects an error with a delayed time and cannot correct the error. Based on the previous system with the delaying technique, other systems have been proposed for timing-error detection and correction in the microprocessor design. They compare an input of a flip-flop and an output of a flip-flop with an XOR gate. By using XOR gates and memory elements, the output is corrected when a fault signal is flagged. Since the time interval is required for the error detection and correction, they return to the normal operation after one clock is sacrificed for the recovery.

Time Borrowing is permitting the logic to automatically borrow time from next cycle or permitting the logic to use slack from previous cycle in current cycle. So, time borrowing is ideally suitable for static logic in a two-phase clocking system latch (non-edge triggered).

Timing Borrow technology, also known as cycle stealing technology, mainly uses the level-sensitive characteristics of latches to obtain data through valid levels and maintain latched data through invalid levels. It is mainly used to solve the situation where the path timing does not meet the circuit requirements. The advantage of time borrowing is that it allows logic between cycle boundaries to use more than one cycle while satisfying the cycle time constraint. Time Borrowing has been traditionally used to reduce the effect of clock skew & jitter on the maximum clock frequency & it also has been widely used in critical delay paths of high-speed circuits especially in high-speed adder designs. Time borrowing can automatically average out delay variations along a path caused by process variations. The input data of the latch should be prepared before the valid edge of the clock, but because the latch is transparent at the valid level of the clock, the data can arrive after the valid edge of the clock, which can be the next clock cycle "Borrow time" (borrow time). It should be noted that once "borrowing time", the time for the subsequent circuit will be reduced.

In modern VLSI circuits, less power and high-speed designs are the essential parameters. To improve the performance of the system it is necessary to enhance the timing elements like latches and Flip-flops. One of the major concerns is the construction of D Flip-Flop (FF) with optimistic power consumption and time delay. The

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most important categories to design any type of electronic system are sequential logic circuits. We already know that D FFs (DFF) are the basic blocks for any type of digital integrated circuits.

2. EXISTING METHOD

Time Borrowing is permitting the logic to automatically borrow time from next cycle or permitting the logic to use slack from previous cycle in current cycle. It always indicates the situation that logic partition in a pipeline structure (flip flops and combinational delays are present between flip flops) use leftover time from the previous stage and this passing of slack time from one cycle to the next cycle is automatic without any additional circuitry or clock adjustments. The time borrowed by the latch from next stage in pipeline is, then, subtracted from the next path's time. This transparent nature allows latches to be used for high-performance designs since they offer more flexibility than edge-triggered circuits in terms of the minimum clock period achievable – a result of time borrowing. Time borrowing happens due to only the latches because latches are level sensitive. Hence, they can capture data over a range of times than at a single time, the entire duration of time over which they are transparent. If they capture data when they are transparent, the same point of time can launch the data for the next stage. Since the use of an edge-triggered structure must require a clock arrival time adjustment at the circuit and this will violate the definition of time borrowing. So, time borrowing is ideally suitable for static logic in a two-phase clocking system latch (non-edge triggered). It extends the time-borrowing and clock-stretching concept proposed in our previous work. The design presented in uses modified master-slave FFs [time-borrowing FF (TBFF)] and an additional clock. The main improvement in this paper from is the elimination of the second clock by using pulsed latches in the critical paths that automatically allow time borrowing. This is realized by developing the LTD circuits (instead of the TBFFs), a time-borrowing detection collector (TDC) circuit considering a single-phase clock, clock pulse generators to realize different time-borrowing window, and an associated clock shifter circuit.

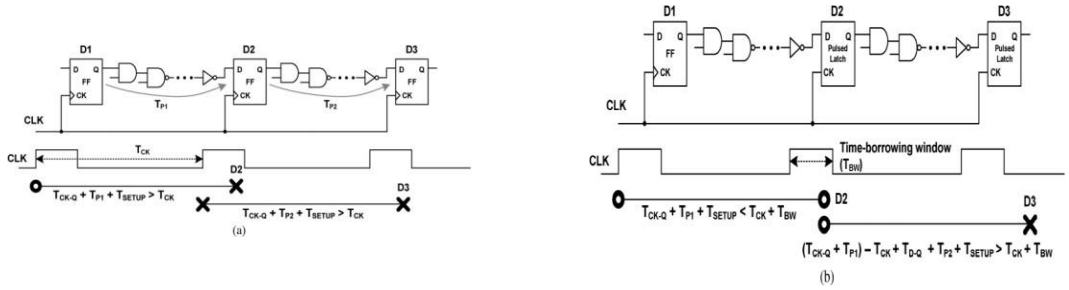

Fig. 1: The Conceptual Operation Of The Pipeline With (A) The Flip-Flops, (B) The Pulsed Latches

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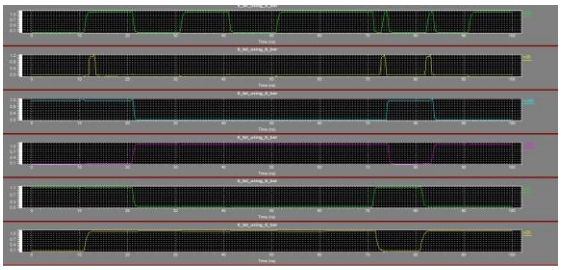

FIG. 2: OUTPUT FOR TIME ERROR TOLERANT CIRCUIT

delay of the latch, and TP2 is the logic delay of stage 2] is greater than the sum of the clock period and time-borrowing window (TCK + TBW) , the pulsed latch in the next stage cannot sample the correct data D3 as shown in Fig. 1(b). Therefore, the pulsed latch with a limited time- borrowing window can prevent timing failures in onestage but cannot in the following stage.

3. PROPOSED METHOD

We propose a timing-error-tolerant method that can correct a timing error immediately through a simple mechanism. In the critical path, the abnormal data

transition after the rising edge of the clock, which is caused by a timing error, is detected, and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowingmethod that copes with the successive errors is introduced. If the timing error occurs in two stages successively, modified CLK in the second stage maintains a transparent window for enough time to make normal data be stored without changing system CLK.

A new timing-error-tolerant system that can correct a timing error is developed. When a timing error causes a delayed arrival of an input on a flip-flop, the proposed

system can detect a delayed input of the flip-flop, and the flip-flop passes through the data by making a transparentwindow.

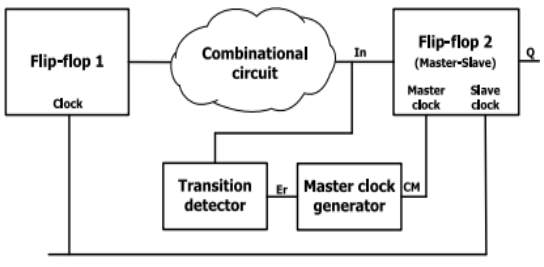

Fig. 3: Circuit diagram of the proposed system

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the proposed system consists of a "transition detector" and "master clock generator." The "transition detector" detects the input transition of a flip-flop, and it produces apulse of the error-flagged signal. Based on the output of the transition detector, the "master clock generator" produces a pulse for a certain period only when a clock is high. While a pulse is "1," the flip-flop passes the input tothe output since the pulse makes a transparent window bycontrolling a clock of master in the flip-flop. Thus, the abnormal data that are stored in the flip-flop can be restored with delayed normal data. To avoid hold time violation, a pulse is generated with a minimum time, which is required for the setup time.

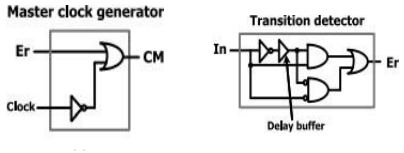

Fig .4: Circuit of transition detector & Circuit of the masterclock generator

The internal circuit of a Transition detector is as shown above. The transition detector consists of an inverter to which the buffer is connected and the output of the buffer is fed to the one of inputs for the gates of AND & BubbledAND while the inputs of these gates are taken from the input. The output of these gates is connected to the OR gates which outputs the error signal. The proposed circuit is implemented with 45 nm process technology. The is performed with the Tanner EDA platform.

This is the internal diagram of Master clock generator. It consists of an OR gate which has the inputs of error signaland clock signal which is connected through inverter. Thisproduces a signal called CM which is given as the input ofclock for Master Latch.

Here the combinational logic used in the design is as shown. It consists of the AND gate and OR gate which have the same inputs and the output of these gates are given to the NAND gates which produces the output for this combinational logic circuit.

When a timing error occurs on the input data of the flip- flop 2, the flip-flop 2 stores abnormal data to the output Q due to the delayed input data. After the delayed normal data have arrived on the input of flip-flop 2, the transition detector that is located between a combinational circuit and the flip-flop 2 generates an error pulse. The transitiondetector detects both a rising edge of the data and a fallingedge of the data by using an inverter and the AND gate. Furthermore, by implementing a delay buffer in the transition detector, the transition detector generates a customized period of a pulse, which maintains the transparent window for enough time. The master clock generator makes a clock of the master (CM) based on the error pulse and clock. Due to the OR gate and inverter in the master clock generator, a CM is high for a certain period after a timing error occurs. While the CM is high, the flip-flop 2 becomes transparent, and the delayed normal input is stored through flip-flop 2. Thus, the erroneous output Q is corrected with the normal input. Since the timing error mostly occurs after a rising edge ofthe clock, the proposed system detects and corrects the timing error, while the clock is high. The proposed methodis applied to the critical paths where the delay of the combinational circuit is longer than the half time of the clock period.

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If a single-stage error occurs, the delayed arriving data signal is recovered because the master latch is transparent for the pulse period. However, if a successive-stage error occurs due to the lack of setup time in the second-stage flip-flop, the delayed arriving data signal in the second stage cannot be stored because of the setup-time violation. To deal with the successive-stage error, we devised the time-borrowing technique. The time-borrowing circuit is provided in the second stage as shown.

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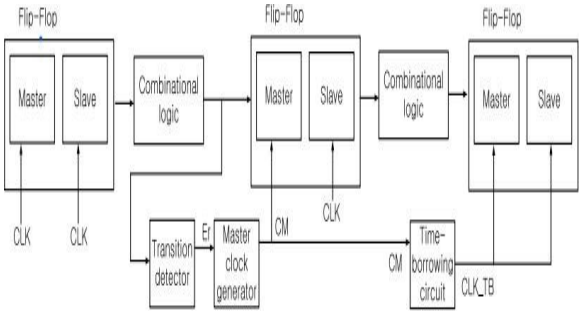

Fig .5: Block diagram of proposed timing error tolerant circuit with time barrowing circuit

In this, an AND gate with one of its inputs connected with NOT gate and the OR gate having same inputs as AND without inverter. The outputs from these gates is given to NOR gate which produces the output of this combinational logic circuit.

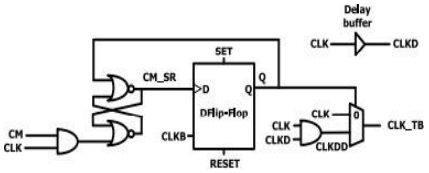

Fig .6: Time barrowing circuit structure

The internal circuit diagram of Time Borrow circuit is shown as above. The operation of a time-borrowing circuit is described as when a timing error occurs on the input data of the first stage,

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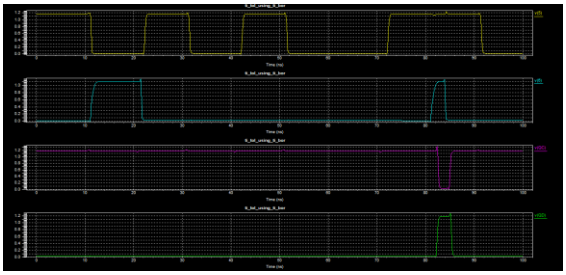

Fig. 7: Outputs For The Proposed System WithTime Borrow Circuit.

the CM signal is set to "1," which also induces the CM_SRhigh level. After CLK is fallen, Q is set to "1." While the Q signal sets the high period, the delayed CLK (CLKDD) is chosen as the main CLK for the second stage. After all,the new CLK maintains a transparent window for enoughtime. A CM is high for a certain period after a timing error occurs. Thus, the delayed data can be stored as normal data. The time-borrowing scheme can be used on any location that has a short setup time for the flip-flop.

CONCLUSION

We propose a timing-error-tolerant method that can correct a timing error immediately with a compact circuit structure. We have presented an effective method to detect and correct timing errors using Timing error tolerant circuit and Tolerant circuit using Time borrowing technique. In the critical path, the abnormal data transitionafter the edge of the clock can be detected and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing technique that deals with the successive-stage error is introduced. If the timing error occurs in the second stage successively, modified CLK maintains the transparent window during enough period for timing-error tolerance without changing system CLK.

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