

PERFORMANCE AND ANALYSIS OF T FLIP FLOP USING CMOS TECHNOLOGY

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ABSTRACT

This paper enumerates low power, high speed design of T Flip-Flop using CMOS technology. The design is implemented by converting D Flip flop to T Flip flop. The designed of T Flip-Flop is compared in terms of its area and power dissipation using DSCH and Microwind tools. As chip manufacturing technology is suddenly on the threshold of major evaluation, which shrinks chip in size and performance is implemented in layout level which develops the low power consumption chip using recent CMOS micron layout tools. The propounded design is the comparison between a flip-flop' auto generated CMOS layout and semicustom layout, which shows the corresponding reduction in power consumption from 57.766 μ W to 43.668 μ W and area is reduced by 13 %.

Keywords: CMOS Technology, D Flip-Flop, T Flip-Flop, VLSI Design

I. INTRODUCTION

Wide utilization of memory storage systems and sequential logic in modern electronics triggers a demand for high-performance and low-area implementations of basic memory components. In these circuits, the output not only depends upon the *current* values of the inputs, but also upon preceding input values. These circuits are often called cyclic logic circuits. These Timing elements (TEs) include latches, flip-flops, registers, and memory storage cells are one of the most important components in synchronous VLSI designs[1,2].

Their performance has a critical effect on cycle time and they often account for a large fraction of total system power. Therefore, there has been significant interest in the development of fast and low power TE circuits, and correspondingly in techniques to evaluate their performance[4].

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems[9]. These have applications which require the temporary retention of one or more bits. Some examples are counters, shift registers, and memories. Bistable circuits can also perform signal shaping functions, e.g., the Schmitt trigger, which exhibits hysteresis and is useful in this regard. The two requirements for realization of bistable operation are amplification (gain greater than unity) and positive feedback. A circuit meeting these requirements can be built using two cross-coupled inverters, as shown in Fig. 1. There are two stable states for this circuit: state 0 is characterized by $Q = 0$ and $Q' = 1$ and state 1 is

characterized by $Q = 1$ and $Q' = 0$ Either state is stable and will be maintained as long as the system power is on; therefore, this circuit can retain 1 bit of information[10,11].

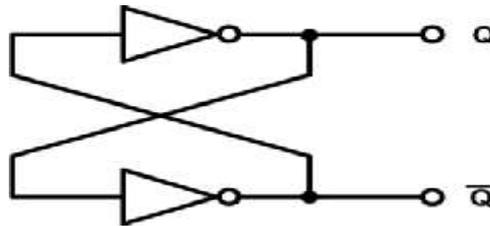


Figure 1: A Bistable Circuit Constructed With Cross-Coupled Inverters

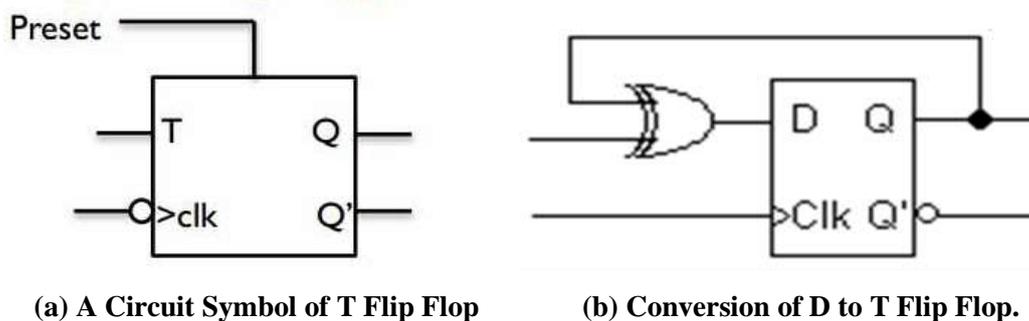
II. T FLIP FLOP

Toggle Flip flop which is also called T Flip flop symbol is shown in fig 2(a). If the T input is high, the T flip-flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip-flop holds the previous value.

This behavior is described by the characteristic equation:

$$Q_{next} = T \oplus Q = T\bar{Q} + \bar{T}Q$$

A T flip flop which is often used for counters can be realized by converting D flip Flop to T Flip Flop. This is accomplished by connecting an Ex-OR gate to the input of D Flip Flop.as shown in figure2(b). All of the popular flip flop can easily be modified to incorporate asynchronous set and/or reset inputs. A T flip flop alternately sends an output signal to two different outputs when an input signal is applied[2,7].



(a) A Circuit Symbol of T Flip Flop

(b) Conversion of D to T Flip Flop.

Figure2. T Flip Flop

Table1: T Flip Flop's Characterstic & Excitation Table

T Flip Flop Operation							
Characteristic Table				Excitation Table			
T	Q	Q _{next}	Comment	Q	Q _{next}	T	Comment
0	0	0	Hold state (no clock)	0	0	0	No Change
0	1	1	Hold state (no clock)	1	1	0	No Change
1	0	1	toggle	0	1	1	Complement

1	1	0	Toggle	1	0	1	Complement

Flip flops operation is illustrated in the above table which shows that T flip flop retain its state when the T is at logic '0', when T is at '1' state output get toggled.

The schematic design of the circuit is shown in figure3 where DSCH 3 is used as a logic editor and simulator.

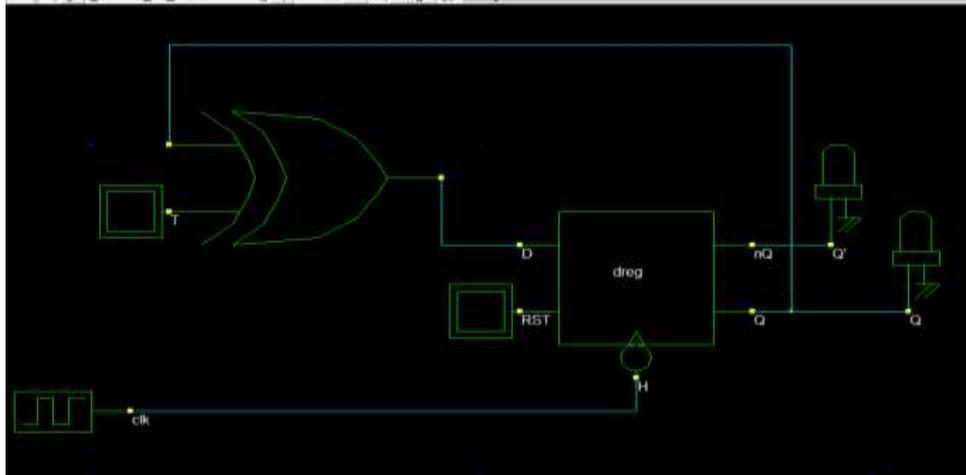


Figure.3 Schematic of T flip-flop

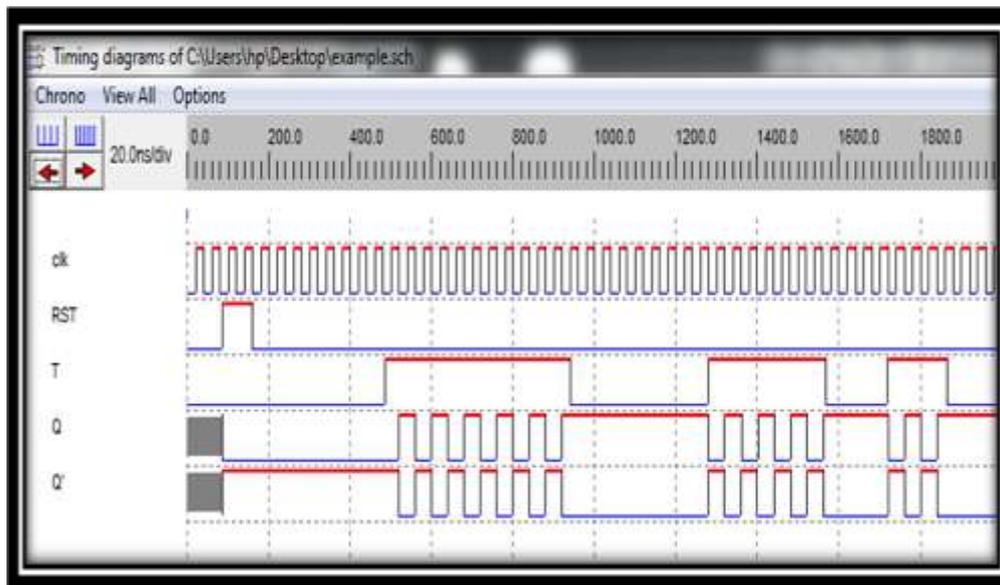


Figure.4: Transient Waveform of T Flip-Flop

III. DESIG OF LOW POWER, HIGH SPEED T FLIP FLOP USING CMOS

This propounded circuit is designed by using strong 1 (pull up) and strong 0 (pull down) transistors namely p-mos and n-mos transistors.

In the below figure, two 3 input NAND gates and two 2 input NAND gates have been used. Whereas out of them 10, n-mos transistors and 10 p-mos transistors, having total of 20 transistors. The efforts are done to give the common V_{dd} supply to reduce the power consumption.

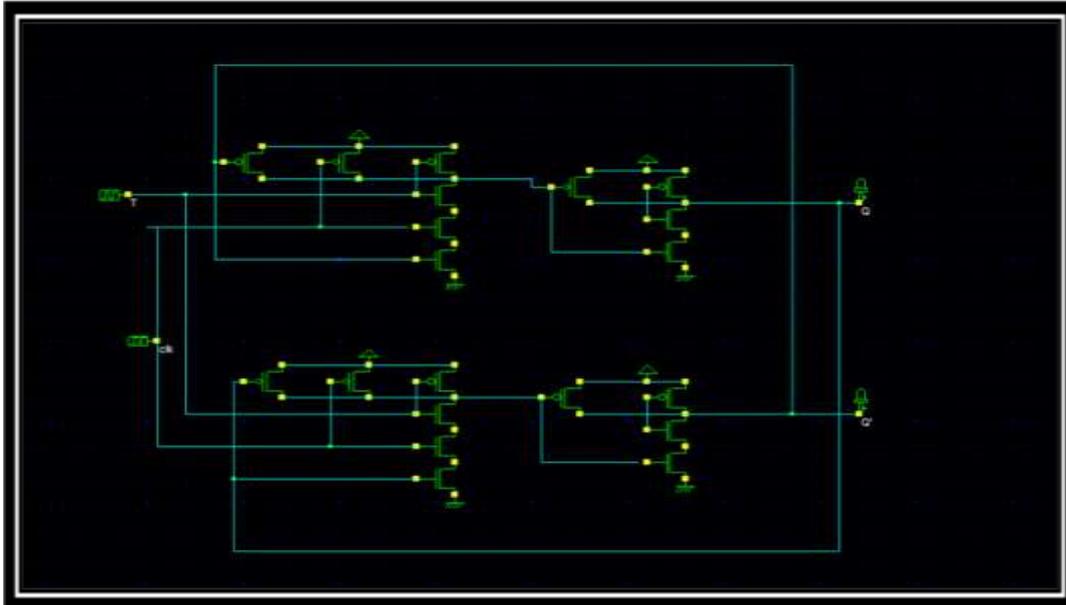


Figure.5: Schematic T Flip Flop in DSCH3

Layout Design Simulation: The first method is the designing of T Flip Flop in DSCH and generating its verilog file. Now in the Microwind this verilog file is compiled and an autogenerated layout is created. So selecting the different foundries available in the library of Microwind software. Here the foundry selected is 180 nm. The layout design of T Flip Flop generated is shown below fig 6.

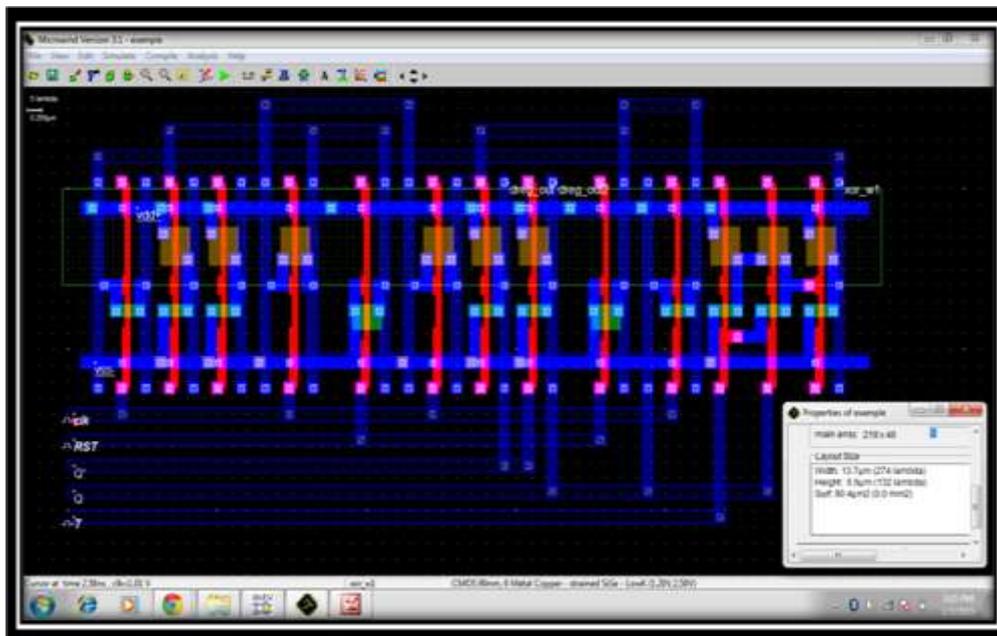


Figure.6: Autogenerated Layout of T Flip Flop

This layout is checked for DRC and if there is no error present, the layout is simulated. The output of the simulation is checked and if the output matches the output of T Flip Flop, then further check out the area and power of this auto generated layout of the circuit.



Figure.7 Simulated Waveforms of Auto Generated Layout of T Flip Flop

Figure 7 shows the simulated waveforms of the layout of fig 6. Simulation results shows that the auto generated layout has area of $90.4\mu\text{m}^2$ and power is $57.766\mu\text{W}$.

The semicustom layout has been generated by using the inbuilt n-mos and p-mos with self-generated metal & poly silicon connections as shown in Figure 8. This design will leads to the less area consumption & low power consumption. When the layout is ready it is checked for the DRC and if there is no error present in the layout, the circuit is simulated and the outputs are obtained. The outputs are verified with the truth table of T Flip flop. After matching of the two further area and power are checked. Sumation result shows that it consume area of $77.2\mu\text{m}^2$ and power consumption is $43.668\mu\text{W}$.

Figure 8 shows the semicustom layout of T Flip Flop and figure 9 shows its simulated input output waveforms

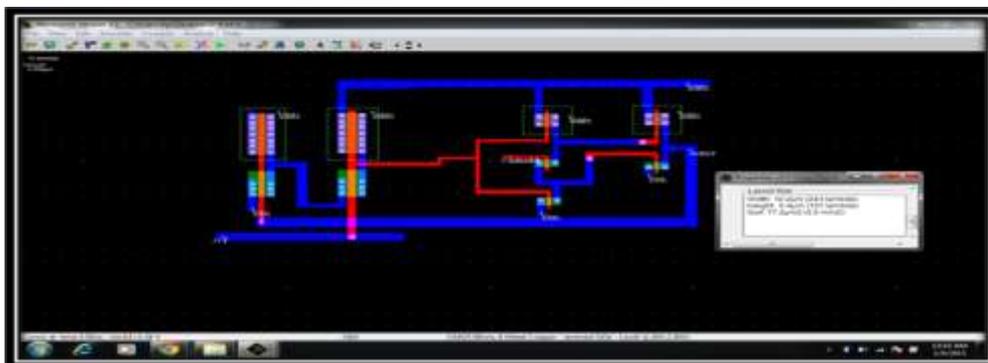


Fig.8 Semicustom Layout of T Flip Flop

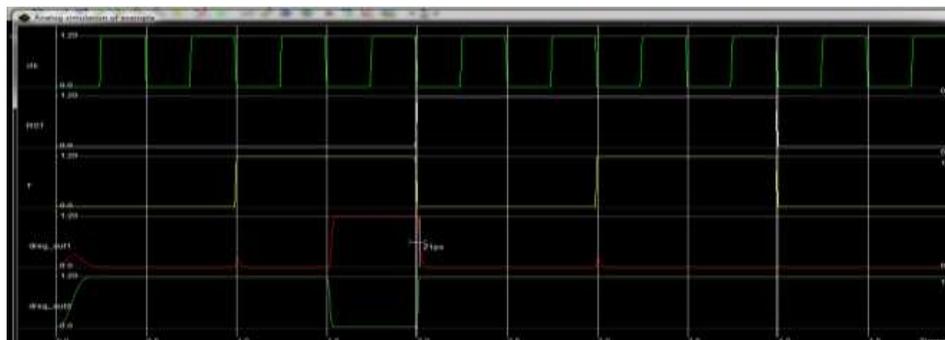


Figure 9 Simulated Waveforms of Semicustom Layout

IV. RESULT AND DISCUSSION

The below table is drawn on the basis of two parameters viz. power consumption & area used. Here analysis has done by comparing the layout of autogenerated and semicustom T flip flops.

Table 2: Comparative analysis of power and area consumption in T Flip Flop.

Parameter considered	Auto generated Layout	Semi Custom layout
Power Consumed	57.766 μ W.	43.668 μ W
Area Consumed	90.4 μ m ²	77.2 μ m ²

A comparative analysis of this table shows that that the area reduced to about 13.2 % and power consumed by the layout reduced to about 14.09% in semicustom layout as compare to auto generated layout of the T flip flop.

V. CONCLUSION

In this paper, an exhaustive analysis and design methodology for T Flip-flop which is made by using D Flip-flop in 90nm CMOS topologies has been carried out. As the most serious problems in VLSI circuit is the area and power dissipation . So comparison has been performed with area and power consumed. The Flip-Flop designed using semicustom generated architecture decreases the power dissipation and area consumed as compared with the auto generated layout . Analysis result shows that the area reduced to about 13.2 % and power consumed by the layout reduced to about 14.09% in semicustom layout as compare to auto generated layout of the T flip flop.

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